What is claimed is

1. A liquid crystal display device comprising:

a liquid crystal display panel;

a plurality of data driver ICs for driving data lines of the liquid crystal display panel;

a first clock signal line for transmitting a first clock signal to the plurality of data driver Ics;

a second clock signal line which is equipped in parallel with the first signal line and transmits a second clock signal which is in reverse relation with the first clock signal;

a timing controller for outputting the first and second clock signals to the first and second clock signal lines respectively; and

load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first clock signal line.

2. The liquid crystal display device according to claim 1, wherein the load means is constructed by equipping dummy terminals to the data driver ICs, and connecting the second clock signal line to the dummy terminals.

3. The liquid crystal display device according to claim 1, wherein the load means is constructed by containing a capacitor in a terminating circuit.

4. The liquid crystal display device according to claim 3, wherein the capacitor has the same capacitance value as the

input capacitance of the first clock signal of the data driver ICs.

5. The liquid crystal display device according to claim 1, wherein a data signal line for odd-number dots for transmitting data signals of odd-number dots and a data signal line for even-number dots for transmitting data signals of even-number dots are equipped, and the timing controller outputs the data signals of the odd-number dots and the data signals of the even-number dots every horizontal line while displacing the phase between the data signals of the odd-number and even-number dots by 180 degrees, and the data driver ICs input the first and second clock signals, latch the data signals of the odd-number dots with the first clock signal and latch the data signals of the even-number dots with the second clock signal.

6. The liquid crystal display device according to claim 5, wherein the timing controller has output pins for the data signals arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.

7. A liquid crystal display device comprising:

a liquid crystal display panel;

a plurality of data driver ICs for driving data lines of the liquid crystal display panel;

a first clock signal line for transmitting a first clock signal to the plurality of data driver Ics;

a second clock signal line which is equipped in parallel with the first clock signal line and transmits a second clock signal which is in reverse relation with the first clock signal; and

a timing controller for outputting the first and second clock signals to the first and second clock signal lines respectively;

wherein the data driver ICs input the first and second clock signals, and can selectively latch data signals with the first or second clock signal.

8. The liquid crystal display device according to claim 7, wherein the data driver IC has input pins for data signals arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.

9. A data driver IC for a liquid crystal display device, characterized in that the data driver IC inputs a first clock signal and a second clock signal in reverse relation with the first clock signal, latches data signals of odd-number dots with the first clock signal and latch data signals of even-number dots with the second clock signal.

10. A data driver IC for a liquid crystal display device, characterized in that the data driver IC inputs a first clock signal and a second clock signal in reverse relation with the first clock signal, and can selectively latch data signals with the first or second clock signal.

11. A timing controller for a liquid crystal display device, characterized in that data signals of odd-number dots and data signals of even-number dots are output every horizontal line while displacing the phase between the data signals of the odd-number dots and even-number dots by 180 degrees.

12. A timing controller for a liquid crystal display device, characterized in that output pins for data signals are arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.